CLAIMS

What is Claimed is:

1. An apparatus for determining whether noise problems potentially will occur on signal lines within an integrated circuit (IC), the signal lines being conductive metal lines in the IC, the apparatus comprising:

first logic, the first logic comparing a signal transition time with a maximum signal transition time constraint for a particular conductive metal line of the IC; and

second logic, the second logic determining whether said signal transition time exceeds said maximum signal transition time, wherein if a determination is made by the second logic that said signal transition time exceeds said maximum signal transition time, a potential noise problem exists with respect to said particular conductive metal line.

2. An apparatus for determining whether noise problems potentially will occur on signal lines within an integrated circuit (IC), the signal lines being conductive metal lines in the IC, the apparatus comprising:

first logic, the first logic determining the maximum length line that can be driven by each driver of the IC and the respective maximum transition time associated with the respective drivers and the respective maximum length lines associated with the respective drivers;

second logic, the second logic determining a transition time for each signal on the IC being driven by respective drivers over respective conductive metal lines of the IC; and

third logic, the third logic determining whether said transition time for each signal exceeds the maximum transition time associated with the driver driving the respective signal over the respective conductive metal line in the IC, wherein if a determination is made that a transition time of a signal exceeds the maximum transition time associated with driver driving the signal, then a determination is made that a potential noise problem exists with respect to the conductive metal line over which the signal having the transition time exceeding the maximum transition time is driven.

3. The apparatus of claim 2, wherein the first, second and third logic correspond to a computer executing a software program that makes the determination of whether a noise problem will potentially occur on a signal line.

4. The apparatus of claim 2, wherein the apparatus is a design tool used during the design of the IC prior to manufacturing the IC.

5. The apparatus of claim 2, wherein the first, second and third logic correspond to separate software routines being executed by a computer, the software routine associated with the first logic being a separate program from the software routines associated with the second and third logic.

6. The apparatus of claim 3, wherein the determinations made by the first and second logic are saved in a memory element accessible by the computer and associated with each other so that stored determinations can be utilized repeatedly by the computer to make the determinations associated with the third logic repeatedly for different IC designs.

7. The apparatus of claim 2, wherein the determinations performed by the first, second and third logic are independent of an IC processing technology used to design the IC.

8. The apparatus of claim 2, wherein a processing technology used to design the IC is a metal oxide semiconductor field effect transistor (MOSFET) technology.

9. The apparatus of claim 1, wherein a processing technology used to design the IC is a complementary metal oxide semiconductor (CMOS) field effect transistor (FET) technology.

10. An apparatus for determining whether noise problems potentially will occur on signal lines within an integrated circuit (IC), the signal lines being conductive metal lines in the IC, the apparatus comprising:

a memory element, for drivers of different sizes, the memory element having maximum transition time constraints stored therein;

a processor in communication with the memory element, wherein for a design of the IC, the processor determines a transition time for each expected signal of the IC design that is to be driven by respective drivers over respective conductive metal lines of the IC, and then determines whether the transition time for each signal exceeds the maximum transition time constraint associated with the driver driving the respective signal over the respective conductive metal line in the IC design, wherein if a determination is made by the processor that a transition time of a signal exceeds the maximum transition time associated with driver driving the signal, a determination is made by the processor that a potential noise problem exists with respect to the conductive metal line over which the signal having the transition time exceeding the maximum transition time is driven.

11. A method for determining whether noise problems potentially will occur on signal lines within an integrated circuit (IC), the signal lines being conductive metal lines in the IC, the method comprising the steps of:

determining the maximum length line that can be driven by each driver of the IC and the respective maximum transition time associated with the respective drivers and the respective maximum length lines associated with the respective drivers;

determining a transition time for each signal on the IC being driven by respective drivers over respective conductive metal lines of the IC; and

determining whether said transition time for each signal exceeds the maximum transition time associated with the driver driving the respective signal over the respective conductive metal line in the IC, wherein if a determination is made that a transition time of a signal exceeds the maximum transition time associated with driver driving the signal, then a determination is made that a potential noise problem exists with respect to the conductive metal line over which the signal having the transition time exceeding the maximum transition time is driven.

12. The method of claim 11, wherein the method is performed by a computer executing a software program that makes the determination of whether a noise problem will potentially occur on a signal line.

13. The method of claim 11, wherein the method is performed by a design tool used during the design of the IC prior to manufacturing the IC.

14. The method of claim 11, wherein each of the determining steps corresponds to a separate software routine being executed by a computer.

15. The method of claim 11, wherein a processing technology used to design the IC is a metal oxide semiconductor field effect transistor (MOSFET) technology and wherein said method is used during the design of the IC.

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16. The method of claim 11, wherein a processing technology used to design the IC is a complementary metal oxide semiconductor (CMOS) field effect transistor (FET) technology and wherein said method is used during the design of the IC.

17. A method for determining whether noise problems potentially will occur on signal lines within an integrated circuit (IC), the signal lines being conductive metal lines in the IC, the method comprising the steps of:

for drivers of different sizes, storing in a memory element associated maximum transition time constraints;

for a design of the IC, utilizing a processor to compare a transition time for each expected signal of the IC design that is to be driven by respective drivers over respective conductive metal lines of the IC with an associated maximum time constraint read by the processor from the memory element, wherein if the result of the comparison is that a transition time of an expected signal exceeds the associated maximum time constraint read out of the memory element the processor determines that a potential noise problem exists with respect to the conductive metal line over which the signal having the transition time exceeding the maximum transition time is driven.

18. A method for determining whether noise problems potentially will occur on signal lines within an integrated circuit (IC), the signal lines being conductive metal lines in the IC, the method comprising the steps of:

comparing a signal transition time with a maximum signal transition time for a particular conductive metal line of the IC; and

determining whether said signal transition time exceeds said maximum signal transition time, wherein if a determination is made that said signal transition time exceeds said maximum signal transition time, a potential noise problem exists with respect to said particular conductive metal line.

19. A computer program for determining whether noise problems potentially will occur on signal lines within an integrated circuit (IC), the signal lines being conductive metal lines in the IC, the computer program being embodied on a computer readable medium, the computer program comprising:

a first code segment, the first code segment comparing a signal transition time with a maximum signal transition time for a particular conductive metal line of the IC; and

a second code segment, the second code segment determining whether said signal transition time exceeds said maximum signal transition time, wherein if a determination is made that said signal transition time exceeds said maximum signal transition time, a potential noise problem exists with respect to said particular conductive metal line.

20. A computer program for determining whether noise problems potentially will occur on signal lines within an integrated circuit (IC), the signal lines being conductive metal lines in the IC, the computer program being embodied on a computer readable medium, the computer program comprising:

a first code segment, the first code segment determining the maximum length line that can be driven by each driver of the IC and the respective maximum transition time associated with the respective drivers and the respective maximum length lines;

a second code segment, the second code segment determining a transition time for each signal on the IC being driven by respective drivers over respective conductive metal lines of the IC; and

a third code segment, the third code segment determining whether said transition time for each signal exceeds the maximum transition time associated with the driver driving the respective signal over the respective conductive metal line in the IC, wherein if a determination is made that a transition time of a signal exceeds the maximum transition time associated with driver driving the signal, then a potential noise problem exists with respect to the conductive metal line over which the signal having the transition time exceeding the maximum transition time is driven.